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24998	7590	02/28/2006	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			TRINH, HOA B	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2814	
DATE MAILED: 02/28/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/002,176

Applicant(s)

YANG ET AL.

Examiner

Vikki H. Trinh

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 32-55,57-65,68,97 and 98 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 32-55,57-65,68,97 and 98 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Objections*

1. Claim 55 is objected to because of the following informalities: In claim 55, line 3, a comma“,” should be inserted **before** the term “and”; In line 4, a comma “,” should be inserted **before** the term “and”. Applicant erroneously amended the claim with the comma **after** the term “and”. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 98 is rejected under 35 U.S.C. 102(e) as being anticipated by Iizuka (6,338,996).

Iizuka discloses a method of forming a capacitor in a semiconductor device , the method including the steps of forming a bottom conducting layer 28 (fig. 1), wherein the bottom conducting layer 28 forms a bottom electrode (col. 3, lines 35-40); forming a dielectric layer 30 (fig. 1) over the bottom conducting layer 28 and annealing the dielectric layer with the first anneal process so as to crystallize the dielectric layer at 1 or 2-10 torr for 40 minutes from 300 up to 700 degrees C (col. 1, lines 30-35; col. 2, lines 13-15; col. 4, lines 55-60); forming a top electrode 32 (fig. 1) that consists of a single top conducting layer (fig. 1) over the dielectric layer

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30; and performing a second annealing process to the single top conducting layer of the top electrode 32 with an oxidizing gas anneal at 1 Too for 40 minutes at 300-400 degrees C (col. 2, line 33; col. Col. 5, lines 20-25).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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7. Claims 32-36, 40-45, 47-49, 51-52, 54, 57-58, 62-63, 97 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka (6,338,996).

Iizuka discloses a method of forming a capacitor in a semiconductor device, the method including the steps of forming a bottom conducting layer 28 (fig. 1), wherein the bottom conducting layer 28 forms a bottom electrode (col. 3, lines 35-40); forming a dielectric layer 30 (fig. 1) over the bottom conducting layer 28 and annealing the dielectric layer with the first anneal process so as to crystallize the dielectric layer (col. 1, lines 30-35; col. 4, lines 55-60); forming a top electrode 32 (fig. 1) that consists of a single top conducting layer (fig. 1) over the dielectric layer 30; and annealing the single top conducting layer of the top electrode 32 with an oxidizing gas anneal (col. 5, lines 20-25). Note that "oxidizing gas anneal" is an anneal performed in a gas mixture with oxygen concentration. Note also that, the first anneal process is used after the dielectric layer is formed so as to crystallize the dielectric layer. The second anneal process is used after the top electrode is formed to recover from any defects after the formation of the dielectric layer (col. 5, lines 25-30). However, Iizuka teaches that annealing process takes about 40 minutes (col. 4, line 29), instead of 10 seconds to 30 minutes as claimed. Nonetheless, as to claim 32, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the annealing period from 10 seconds to 30 minutes, since it is a prima facie of obvious to an artisan for optimization and experimentation to limit the annealing period to a range of 10 seconds- 30 minutes because applicants have not yet established any criticality for the range. Note that in the specification, page 5, line 5, applicants state that the annealing period is from 10 seconds to 60 minutes.

*Lastly, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)*

As to claim 33, Iizuka discloses that the capacitor is formed over a conductive plug 18 (fig. 1) or 21 (fig. 2b), and further includes depositing an oxygen barrier 24 or 26 (fig. 1) over the plug 18 or 21 (fig. 1 or fig. 2b) prior to forming the bottom conducting layer 28 (fig. 1).

As to claim 34, Iizuka discloses that the step further includes annealing the dielectric layer after the dielectric layer is formed (col. 4, lines 55-60).

As to claim 35, Iizuka discloses that the bottom conducting layer 28 (fig. 1) is formed of a material selected from the noble metal group (col. 3, lines 38-40).

As to claim 36, Iizuka discloses that the bottom conducting layer is formed of a metal (col. 3, lines 38-40).

As to claims 40-41, Iizuka discloses that the bottom conducting layer is formed from material such as platinum (Pt) and Ruthenium (Ru). (col. 3, lines 38-40).

As to claim 42, Iizuka discloses that the dielectric layer is a dielectric metal oxide layer (col. 3, lines 40-42).

As to claim 43, Iizuka discloses that the dielectric layer has a high dielectric constant that falls within the range as claimed. (e.g. BST, Col. 3, lines 40-42).

As to claims 44-45, Iizuka discloses that the dielectric layer 30 (fig. 1) is formed of a material such as BST. (Col. 3, lines 40-42).

As to claim 47, Iizuka teaches that the dielectric layer 30 (fig. 1) is heated to a temperature above 200 degrees Celsius (col. 4, lines 59-60) to change it to a crystallized dielectric layer 30 from an original material that may be an amorphous material (col. 4, lines 55-63, col. 1, lines 30-33). Note that Applicants disclose the same material BST for the dielectric layer as that of Iizuka. Thus, the change of the BST material from the annealing process has the same effect as that of applicants.

As to claim 48, Iizuka discloses that the top conducting layer 32 (fig. 1) is formed of a material selected from the noble metal group (col. 3, lines 38-40).

As to claim 49, Iizuka discloses that the top conducting layer 32 is formed of a non-oxidizing metal permeable to oxygen (col. 3, lines 38-40).

As to claims 51-52, Iizuka discloses that the top conducting layer 32 (fig. 1) is formed from material such as platinum (Pt) and Ruthenium (Ru). (col. 3, lines 38-40).

As to claim 54, Iizuka discloses that the top and bottom conducting layers 32, 28 (fig. 1) are formed of a material such as platinum (col. 3, lines 38-40) and the dielectric layer 30 (fig. 1) is a BST (col. 3, lines 40-42).

As to claims 57-58, Iizuka discloses that the annealing is performed with a gas mixture having a material such as oxygen (col. 5, lines 20-25).

As to claims 62 and 63, Iizuka teaches that the annealing is performed at a temperature between 300-400 degrees Celsius (col. 2, line 44), which falls within the claimed range.

As to claim 97, Iizuka discloses the invention substantially as claimed, except that the range for annealing the top electrode is from 300-400 degrees C which is below claimed range of greater than 400 degrees C. Nonetheless, it would have been obvious to one of ordinary skill in

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the art at the time the invention was made to modify the invention of Iizuka with the annealing range greater than 400 degrees C, since it is a prima facie of obvious to an artisan for optimization and experimentation to select a range of temperature for annealing the top electrode because applicants have not yet established any criticality for the range. Note that in the specification, applicants state that the annealing range is performed at 300 to 800 degrees C. (specification, page 5, line 6).

1. Claims 37-38 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka, as applied to claim 32, in view of Emesh et al. (5,452,178) (hereinafter Emesh).

Iizuka discloses the invention substantially as claimed. However, Iizuka does not explicitly state that the bottom conducting layer may be formed of a metal alloy or conducting metal oxide, and that the top conducting layer is formed of a conducting metal oxide.

Emesh discloses an analogous method and device having a bottom electrode 54 (fig. 3), a dielectric 60, 64 (fig. 3) , and a top electrode 68 (fig. 3) , wherein the bottom electrode 54 (fig. 3) may be formed of conductive metal alloy, or conductive metal oxide (col. 7, lines 1-2). The top electrode 68 may be formed of conducting metal oxide (col. 9, lines 40-42).

Therefore, as to claims 37-38, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bottom electrode of Iizuka with the metal alloy or conductive metal oxide material, as taught by Emesh, so as to provide an alternative material to make the bottom electrode.

As to claim 50, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the top electrode made of



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conductive metal oxide, as taught by Emesh, so as to provide an alternative material to make the top electrode.

2. Claims 39, 46, 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka, as applied to claim 32, in view of Alers (6,303,426).

Iizuka discloses the invention substantially as claimed. In particular, Iizuka discloses that the top conducting layer 32 (fig. 1) is formed of platinum (Pt). However, Iizuka does not explicitly state that the bottom conducting layer may be formed of a metal nitride and the dielectric layer may be formed of a Tantalum oxide (TaO) and is crystalline or amorphous material.

Alers discloses an analogous method and device having a bottom electrode 66 (fig. 3), a dielectric layer 70 (fig. 3), and a top electrode 80 (fig. 3), wherein the bottom electrode 66 is made of metal nitride material (col. 3, lines 53-54) and the dielectric layer 70 is formed of Tantalum Oxide (TaO) and is either crystalline or amorphous (col. 3, lines 58-65).

Therefore, as to claims 39 and 53, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the bottom electrode made of metal nitride, as taught by Alers, so as to provide an alternative material for the bottom electrode.

As to claim 46, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the dielectric layer made of Tantalum oxide (TaO), as taught by Alers, so as to provide an alternative material for the dielectric layer.

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3. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka, as applied to claim 32, in view of Alers (6,303,426), and further in view of Emesh et al. (5,452,178) (hereinafter Emesh).

Iizuka discloses in the invention substantially as claimed. In particular, Iizuka discloses that the top conducting layer 32 (fig. 1) is formed of platinum (Pt). However, Iizuka does not explicitly state that the bottom conducting layer is a tungsten nitride and the dielectric layer is an aluminum oxide ( $\text{Al}_2\text{O}_3$ ).

Alers discloses an analogous method and device having a bottom electrode 66 (fig. 3), a dielectric layer 70 (fig. 3), and a top electrode 80 (fig. 3), wherein the bottom electrode 66 is made of tungsten nitride (WN) (col. 3, lines 53-55) and the dielectric layer 70 is formed of Tantalum Oxide (TaO) and is either crystalline or amorphous (col. 3, lines 58-65).

Emesh discloses an analogous method and device having a bottom electrode 54 (fig. 3), a dielectric 60, 64 (fig. 3), and a top electrode 68 (fig. 3), wherein the dielectric layer is formed from material such as silicon dioxide (col. 8, line 40), PZT (col. 8, line 59), or  $\text{Al}_2\text{O}_3$  (col. 9, line 27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the bottom electrode made of tungsten nitride material, as taught by Alers, so as to provide an alternative material for the bottom electrode. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the material for the dielectric layer of Iizuka with the aluminum oxide ( $\text{Al}_2\text{O}_3$ ) material, as taught by Emesh, so as to provide an alternative material for the dielectric layer.

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4. Claims 59-60, 64-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka, as applied to claim 32, in view of Narwankar et al. (6,475,854) (hereinafter Narwankar).

Iizuka discloses the invention substantially as claimed. However, Iizuka does not explicitly disclose that the annealing step is a plasma enhanced annealing, a remote plasma enhanced annealing, or ultraviolet light enhanced annealing, and that the annealing is performed at a pressure between 2-660 Torr and between 10 seconds to 60 minutes.

Narwankar discloses an analogous method and device having a bottom electrode 604 (fig. 6f), a dielectric layer 606 (fig. 1), and a top electrode 610 (fig. 6f), wherein the top electrode 610 is annealed (col. 11, line 4-5) in an oxygen environment, thereby performing an oxidizing annealing step. The annealing is a plasma enhanced annealing, or remote plasma enhanced annealing (col. 13, lines 14-20) and that the annealing is done at a pressure of 2.5 Torr and performed at 2 minutes (col. 13, lines 10-15).

Therefore, as to claims 59-60, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with the annealing such as plasma enhanced annealing, or remote plasma enhanced annealing, as taught by Narwankar, so as to provide an alternative technique to anneal the top electrode.

As to claims 64-65, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Iizuka with a pressure of 2.5 Torr (which falls within the claimed range of the pressure), as taught by Narwankar, so as to provide a pressure for annealing the top electrode layer.

As to claims 66-67, Narwankar teaches that annealing is performed for 2 minutes (which falls within the claimed range for time duration) because the time duration is depended on the particular oxygen –containing environment (col. 9, lines 63-66).

As to claim 68, Iizuka and Narwankar teach the invention substantially as claimed. However, neither Iizuka nor Narwankar teaches a gas flow rate between .01-10 liters per second. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teaching of Iizuka and Narwankar with a specific range for the gas flow rate as claimed, since it is a prima facie obvious to an artisan for routine experimentation and optimization to set a specific range for the gas flow rate because applicants have not yet established any criticality for the specific range. *Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. (In re Woodruff, 919 F.2d 1575, 1578 (Fed. Cir. 1990).)*

5. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iizuka, as applied to claim 32, in view of Marsh (6,387,802).

Iizuka discloses the invention substantially as claimed. In particular, Iizuka discloses the top electrode 32 made of platinum (Pt) (col. 3, lines 38-39). However, Iizuka does not explicitly teach that the annealing step of the top electrode is an ultraviolet light enhanced annealing.

Marsh discloses an analogous method and device having a bottom electrode 152 (fig. 11), a dielectric layer 153 (fig. 11), and a top electrode (col. 8, lines 30-35), wherein the top electrode

is deposited and annealed (col. 2, lines 30-35) using ultraviolet light enhanced annealing in the same manner as the bottom electrode.

Therefore, as to claim 61, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the annealing step of Iizuka with ultraviolet light enhanced annealing, as taught by Marsh, so as to provide an alternative technique to anneal the top electrode and to remove carbon in the platinum group metal of the top electrode (col. 2, lines 34-35).

#### ***Response to Arguments***

6. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

#### **Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

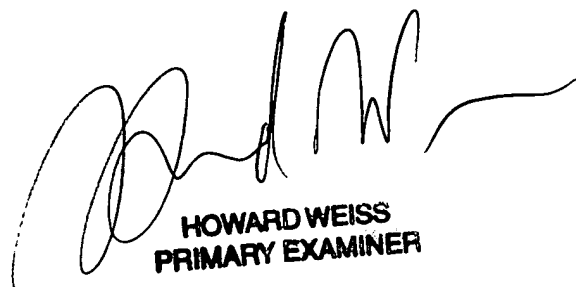
Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspro.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at

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<http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,  
Patent Examiner  
AU 2814



**HOWARD WEISS**  
**PRIMARY EXAMINER**